nesses of silicon, Si_3N_4 and W layers. This was a result of absorption of radiation in the layers, modified by the interference due to internal reflections in the structure. The time constants ranged from 1 to 7 ms for devices operated in air. Thermal capacitance per unit of area was dependent on thickness of the silicon and silicon nitride layers, ranging from 4×10^{-5} JK^{-1}cm^{-2} to $\approx2\times10^{-4}$JK^{-1}cm^{-2}. This can be reduced using thinner membranes and silicon layers and improve performance at high frequencies.

Detectivities up to 10^8 cmHz$^{1/2}$/W were measured at low frequencies (≈20 Hz) for the best devices operated in Kr-Xe mixtures. The detectivity decreases with increasing frequency due to decreasing voltage responsivity. The decrease of voltage responsivity is, in some degree, compensated by the excess noise reduction.

Similar micromachined bridge structures has been used for thermal microemitters of infrared radiation. Much stronger doping has been used to obtain sheet resistances of ≈1 kΩ/sqr. This was necessary for low voltage power supply to few volts. Another advantage of high doping is a low TCR. The devices exhibited integral luminance of 10 mW/(mm^{2}srd). The spectral luminance peaked in the range of 3-5 μm with values higher than that achieved with ≈4 μm LEDs operated at room temperature. The shape of spectral luminance can be modified by selecting thickess of the Si, Si_3N_4 and W layers to establish resonant optical resonance in required spectral range. The response time was 1-4 ms, decreasing with increased bias. This enables to modulate luminance changing electrical bias.

Improved performance and reliability with the reduced cost associated with silicon micromachining technology and compatibility with standard IC make the bolometers and thermal emitters attractive for many high-volume civilian and military applications, such as non-contact thermometry, gas analyzers, exhaust-emission controls and medical monitor instrumentation.

Short biography note

Józef Piotrowski received his PhD in 1973 from Military University of Technology, Warsaw, Poland. His scientific interests concern semiconductor physics and technology, IR physics, microelectronics and optoelectronics. He was engaged in the research and design of infrared photodetectors based on II-VI and III-V narrow gap semiconductors. He has developed and introduced into practice many types of novel IR photodetectors operating without cooling. Currently he is a development manager of VIGO SYSTEM Ltd. Warsaw. Author or co-author of about 200 papers and monographs on infrared photodetectors.

Lech Dobrzański was born in Starachowice, Poland, in 1951. He received M.Sc. degree from Warsaw Technical University in 1974. From 1974 to 1988 he worked in Scientific & Production Center CEMI. He was involved as a leader of the technological team in a project of LEDs on GaAsP (from 1974 to 1979). The successful set up of production line was awarded in 1978. From 1980 to 1985 he was involved in a project of polish microprocessor chip. Project was completed in 1984 and awarded. From 1995 to 1988 he worked at CEMI as a designer of bipolar integrated circuits. In 1988 he joined ITME. Here he was involved in organization of a laboratory for making semiconductor devices on $A_{III}B_V$. In 1994 he received Ph.D. degree from ITME. His research interests include modelling of technology, modelling of semiconductor devices and ICs.

SILICON FOR MST APPLICATIONS

Elżbieta Nossarzewska-Orłowska
Piotr Zabierowski

At the present time demand for the silicon wafers, suitable for use in the production of sensors, is increasing rapidly. Material for the sensors often has to fulfil a number of particular requirements, which in many cases needs a tailor made technology and solving problems of specific nature for, what are mainly, short production series. Parameters, listed below, may be required, depending on the type of sensor, as a combined or a single feature.

In monocrystals:

- Low radial resistivity variation combined with the necessity of obtaining uniform distribution of dopants in the monocrystal (need to conduct the process with as flat as possible front of crystallisation).
- Material of perfect crystallographic structure (free from swirls, with dislocations density lower than given by SEMI standard - 500/cm^2).

In wafers:

- Orientation tolerance better than ±0.25°.
- Very good polishing surface (polishing is special and very slow).
- Wafers of varying thicknesses, polished on one or both sides depending on technology and the type of sensor. In demand are wafers both very thin (50÷70 μm) and very thick (for example 5000 μm ±25 μm).
- Wafers of various, often nonstandard diameters.
- Very precise orientation of flats. Very often there are required wafers of special geometry, depending on application.
- Bow down to 10 μm.
- TTV down to 5÷8 μm.
- Thickness tolerance ±5 μm (standard tolerance ±25 μm).

Table 1. Technical parameters of Si wafers for MST.

Diameter [mm]	50.8 ± 0.3	76.0 ± 0.5	100 ± 0.5
Orientation	<100>	<100>	<100>
Thickness [μm]	40÷5000	60÷5000	70÷5000
Thickness tolerance [μm]			
max	7	7	10
typical	5	5	7
Total thickness variation [μm]			
TTV max	5	7	8
Diameter [mm]	50.8 ± 0.3	76.0 ± 0.5	100 ± 0.5
Orientation	<111>	<111>	<111>
Thickness [μm]	40÷5000	70÷5000	80÷5000
Thickness tolerance [μm]			
max	7	7	10
typical	5	5	7
Total thickness variation [μm]			
TTV max	5	7	8

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Parameters given in the Table 1 cover values most often met in enquiries for wafers for applications in microsystems. The equipment possessed by ITME and the skill and knowledge of its employees make it possible to satisfy these requirements.

In addition, ITME is conducting research with an aim of working out the technology of direct bonding (thermal bonding) of silicon wafers. Method of thermal bonding enables to bond two or more wafers having oxydised or monoxydised surfaces.

Some of this materials are already used by the industry for the design of various sensors (especially pressure and acceleration sensors). It is expected that these new materials will enable a broad sensor range of novel design and high performances.

In epitaxial wafers:

Research has also been conducted on epitaxial silicon layers technology.

Table 2. Technical data of silicon epitaxial layers on monocrystalline substrates. Epilayers are phosphor or boron doped.

Wafer diameter [mm]	50.8 ± 0.3	76.0 ± 0.5	100 ± 0.5
Epilayer thickness [μm]	1 ÷ 100 (± 10%)		
Epilayer resistivity [Ωcm]	1 ÷ 300 (± 15%)		
Orientation	<100>		

Silicon epitaxial layers are deposited on silicon monocrystalline substrates by means of CVD process. $SiCl_4$ is used as a silicon source and PH_3, B_2H_6 - as dopants.

Technical parameters for the epitaxial layers are given in the Table 2.

High resistivity layers for application in radiation sensors were developed. An example of resistivity distribution in such a layer is given in Fig.1

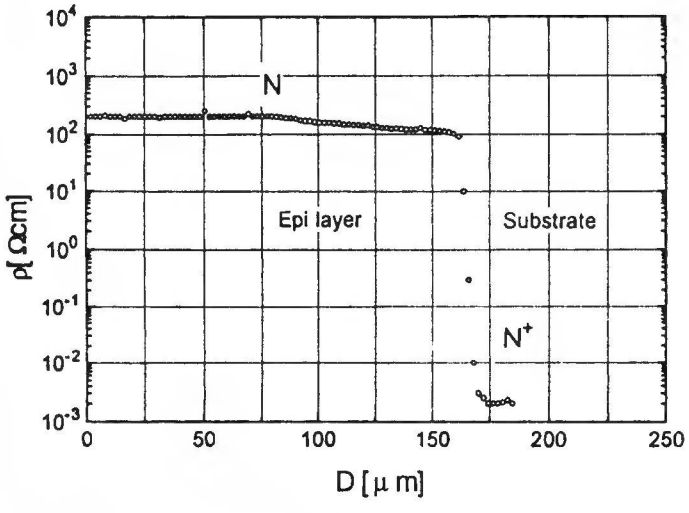

Fig.1. Resistivity distribution in a thick, high resistivity epitaxial layer.

In porous silicon:

The technology of porous silicon formation by anodization in HF-based electrolyte was elaborated. Epitaxial Si layers on porous silicon by CVD method can also be deposited (see Fig.2)

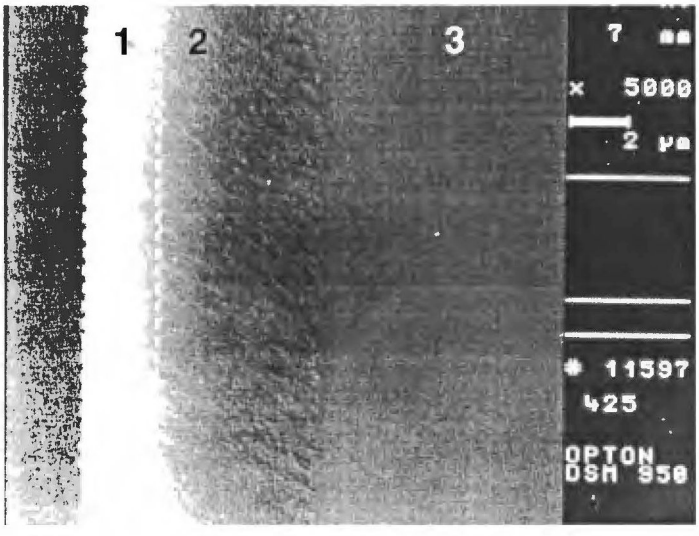

Fig.2. SEM picture on a cleaved wafer with epitaxial monocrystalline layer on porous silicon.
1 - epitaxial layer (thickness 2.32 μm)
2 - porous layer (thickness 5.12 μm)
3 - p^+<111>Si substrate.

Technical data of silicon epitaxial layers on porous silicon are given in Table 3.

Table 3. Technical data of silicon epitaxial layers on porous silicon formed in p^+ (about 0.01Ωcm) monocrystalline wafers.

Wafer diameter [mm]	50	76
Porosity [%]	30 ÷ 60 (± 10%)	30 ÷ 50 (± 10%)
Porous layer thickness [μm]	1 ÷ 30 (± 5%)	1 ÷ 30 (± 5%)
Epilayer thickness [μm]	1 ÷ 5 (± 20%)	1 ÷ 5 (± 20%)
Defects density in epilayer [cm^{-2}]	10^4 ÷ 10^5	

The porous silicon under the epitaxial monocrystalline layer can be used as a sacrificial layer, or being oxidised can act as an insulator.

Short biography note

Elżbieta Nossarzewska-Orłowska received her PhD degree in chemistry in 1973 from the Institute of Physical Chemistry of Polish Academy of Science, Warsaw. In 1972 she joined the Institute of Electronic Materials Technology where she has organized a research group working on epitaxial growth of semiconductors (Epitaxy Department since 1975). Under her leadership a production of silicon epitaxial wafers has been established. In 1992 she initiated a work on porous silicon in the Institute.

Piotr Zabierowski was born in 1945 in Gorlice (Poland). He obtained M.Sc. at the Academy of Mining and Metallurgy of Cracow in non-iron metals metallurgy (plastic working and metal science) in 1968. He works as head of Silicon Technology Department in the Institute of Electronic Materials in Warsaw. His research work concern recently technology of growth of silicon and Si_xGe_{1-x} single crystals and silicon wafer thermal bonding.