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CHARACTERIZATION OF EPITAXIAL SILICON FOR MOS VLSI IC BY DEEP LEVEL TRANSIENT SPECTROSCOPY AND MINORITY CARRIER LIFETIME MEASUREMENTS

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The effect of silicon source contamination on the properties of epitaxial layers was studied by DLTS technique and generation lifetime measurements. The influence of substrate etching procedure on the generation lifetime is also shown.

Introduction

Epitaxial silicon is widely used as starting material for small geometry CMOS devices. However, during the epitaxial growth a variety of native defects and impurities are introduced into the layers. When located in the active region of devices, these point defects, particularly transition metal impurities, have strong detrimental effect on the device performance. So, for the quality assessment of epitaxial silicon for MOS VLSI integrated circuits it is necessary to control the type and concentration of point defects as well as the minority carrier lifetime.

In this paper we present the results of characterization of epitaxial silicon by deep level transient spectroscopy (DLTS) and measurements of the generation carrier lifetime in MOS structures.

Experimental procedure

The p^+ and n^+ starting substrates for epitaxy were 100mm diameter CZ wafers with <111> orientation. The p^+ wafers were boron doped with the resistivity in the range of 0.01-0.02 Ωcm. The n^+ wafers were antimony doped with the resistivity in the range of 0.008-0.018 Ωcm.

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The wafers were prepared by standard lapping, wet etching and polishing processing. In the case of the n^+ substrate two different types of chemical etchant have been used:

- acid solution, consisted of HNO_3, HF and CH_3COOH,
- alkaline solution, consisted of KOH and stabilizers.

All the other mechano-chemical treatments, including final cleaning were identical for all substrates.

The epitaxial layers were deposited in a rf heated Gemini 1 reactor of vertical type with rotated pancake-like graphite susceptor. An in-situ HCl etching at 1180°C was used to remove about 1μm of the silicon layer prior to the deposition. The epitaxial deposition was performed at 1120°C with the growth rate of 1μm/min.

Two silicon sources were used for epitaxial growth: $SiCl_4$ and $SiHCl_3$. As dopants 25vpm B_2H_6 in H_2 was used for the p-type layers and 25 vpm PH_3 in H_2 for the n-type layers.

In the test processes, performed without intentional doping, the resistivity of layers grown from $SiCl_4$ was 180 Ωcm and 800 Ωcm in the case of using $SiHCl_3$.

The layer thickness was measured by means of a standard infrared reflection spectrophotometer. The resistivity was determined by spreading resistance method.The majority carrier concentration profiling by C-V method with Hg probe was also made.

For the carrier generation lifetime measurement the gate silicon oxide of 1000 Å thickness was deposited on the layer surface. The electrical contact to the oxide was made by means of Hg probe of 1mm diameter. The value of carrier lifetime in the obtained MOS structures was calculated by Zerbst method.

The measurements were performed using computer-controlled CSM/16 System with Hg probe (Materials Development Corp.).

DLTS measurements were performed on Schottky diodes fabricated by Au evaporation onto the surface of epitaxial layers. Measurements were carried out by a standard DLS 81 equipment. Temperature scans were performed for various rate windows (2 - 2000 s^{-1}) with increasing temperature in the range of 80 300K and the

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temperature dependence of the carrier emission rate $e_n = f(T)$ was determined. The reverse bias was -10V and filling pulse amplitude was equal to 9V. The energy levels were determined from Arrhenius plots $\ln(e_n/T^2)$vs 1/T. The deep centre concentration N_T was calculated from the well-known relation [1]:

$$N_T = 2\Delta C(N_D - N_A)/C_{st}$$

where ΔC is the DLTS output, C_{st} is the quiescent capacitance of the reverse-biased diode and N_D-N_A is the majority carrier concentration.

Experimental results and discussion

The main purpose of our studies was to show how the uncontrolled impurities affect the quality of the epitaxial layers.

In the first experiment the epitaxial layer of 10 μm thickness and 10 Ωcm resistivity were deposited from two silicon sources of different test resistivity. According to the results presented in Table 1, in both types of epistructures (n/n^+ and p/p^+) the source contamination influence on the carrier generation lifetime is clearly seen.

Table 1. Dependence of τ_g on silicon source used for epitaxy.

Structure	Silicon source	Gen. lifetime τ_g[μs]
n/n^+	$SiCl_4$ - test resistivity 180 Ωcm	65
	$SiHCl_3$- test resistivity 800 Ωcm	115
p/p^+	$SiCl_4$ - as above	300
	$SiHCl_3$- as above	400

The DLTS spectra for epitaxial layers deposited from $SiCl_4$ and $SiHCl_3$ are shown in Fig.1 and Fig.2 respectively. The Arrhenius plots for deep-level deffects detected in the epitaxial layers are presented in Fig. 3.

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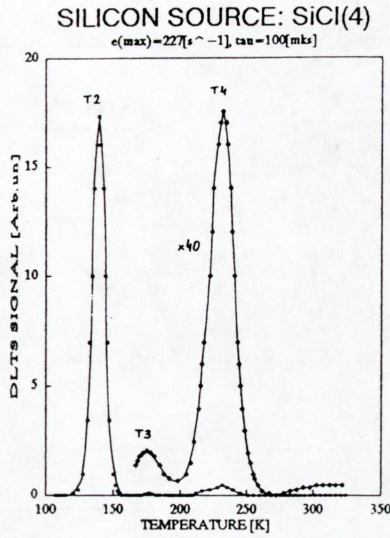

Fig.1. DLTS spectrum for epitaxial layers deposited from $SiCl_4$.

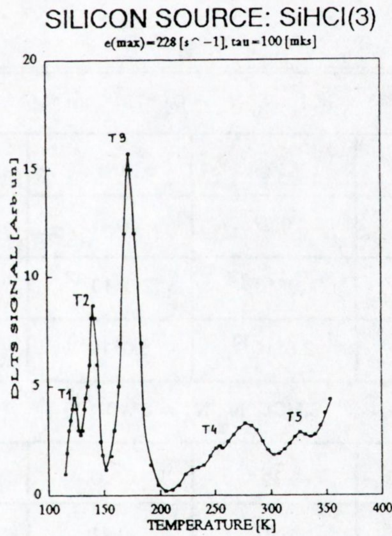

Fig.2. DLTS spectrum for epitaxial layers deposited from $SiHCl_3$.

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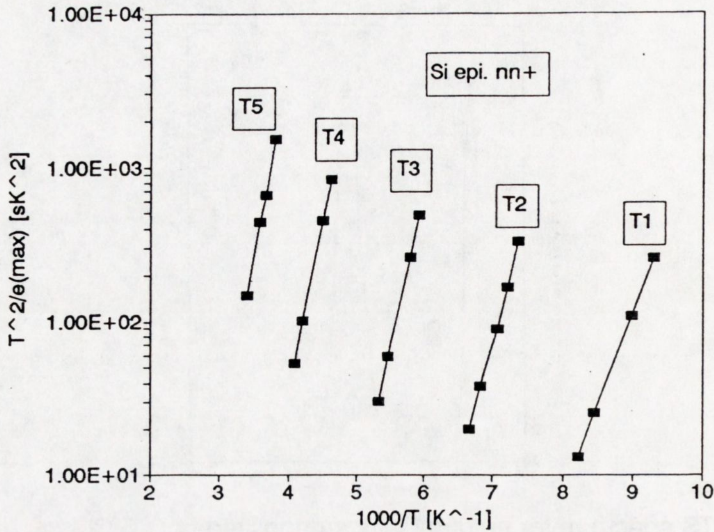

Fig.3. Arrhenius plots for deep-level defects detected in the epitaxial layers grown from $SiCl_4$ and $SiHCl_3$.

Table 2. Parameters of deep traps detected in epitaxial layers grown from $SiHCl_3$ and $SiCl_4$.

$SiCl_4$, N_D-N_A = 9.6*10^{13}[cm^{-3}]					
Trap	T_1	T_2	T_3	T_4	T_5
E_a[eV]	-	0.27	0.41	0.56	-
σ_a[cm^{-3}]	-	1.0*10^{-13}	2.0*10^{-12}	4.0*10^{-12}	-
N_T[cm^{-3}]	-	2.8*10^{13}	8.0*10^{10}	7.0*10^{11}	-
$SiHCl_3$, N_D-N_A = 3*10^{12-3}]					
Trap	T_1	T_2	T_3	T_4	T_5
E_a[eV]	0.24	0.27	0.41	0.56	0.68
σ_a[cm^{-2}]	6.0*10^{-13}	1.3*10^{-13}	2.0*10^{-12}	4.0*10^{-12}	6.0*10^{-12}
N^T[cm^{-3}]	9.0*10^{9}	1.6*10^{10}	2.8*10^{10}	1.8*10^{9}	6.0*10^{9}

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The results of the silicon source characterization obtained from DLTS measurements are presented in Table 2.

According to the data presented in Table 2 the concentration of deep traps in the epitaxial layers deposited from $SiHCl_3$ is by three orders of magnitude lower than in that obtained from $SiCl_4$. These traps are likely to be atributed to transition metal impurities [2].

In the second experiment the epitaxial layers were grown on the n^+ substrates prepared by alkaline etching as well as by acid etching. The influence of the residual alkaline ions in the n type epitaxial layers on the carrier lifetime is shown in the Table 3. As alkaline ions result in decreasing carrier lifetime, substrates for the high epitaxy standard should be etched in the acid solution.

Table 3. Dependence of τ_g on substrate chemical etching.

Layer parameters		Generation lifetime, τg [μs]	
Thickness [μm]	Resistivity [Ωcm]	Acid etching	Alkaline etching
9.5	3.5	45	22
18.5	47.0	150	30

Conclusions

The carrier generation lifetime measurements on MOS epitaxial structures can be used as a criteria of the quality of epitaxial layers.

The DLTS measurements give additional useful information on the properties and concentration of deep traps. So, DLTS is also powerful tool for quality characterization of materials used in the epitaxy processes.

According to the obtained data, uncontrolled impurities in epitaxial layers are mainly introduced from the source of silicon used for epitaxy. Substrate etching in alkaline solution have to be avoided in the MOS VLSI production.

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Od redakcji:

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